AMENDMENT TO THE CLAIMS

1. (Currently Amended) A system for detecting a synchronization (sync) signal in a communication signal, comprising:

a memory configured to store consecutive portions of a received communication signal; and

a sync signal detector configured to read the ~~consecutive~~ stored consecutive portions of the received communication signal from the memory, monitor the read stored consecutive portions of the received signal to detect the sync signal, and determine whether or not the sync signal detected in the read stored consecutive portions of the received communications signal is invalid, wherein the sync signal detector reads and monitors previously read stored consecutive portions of the received communications signal from the memory when the detected sync signal is invalid.

2. (Currently Amended) The system of claim 1, further comprising a signal processor configured to read and process stored consecutive portions of the received communication signal which are stored in the memory following the detected sync signal.

3. (Original) The system of claim 2, wherein the sync signal detector is configured to monitor an output signal from the signal processor to determine if the detected sync signal is invalid.

4. (Original) The system of claim 3, wherein the sync signal detector monitors an error rate of the output signal of the signal processor and determines that the detected sync signal is invalid if the error rate exceeds a threshold.

5. (Original) The system of claim 2, wherein processing operations of the signal processor are discontinued when the sync signal detector determines that the detected sync signal is invalid.

6. (Original) The system of claim 2, wherein:

the communication signal comprises a plurality of frames; and

the sync signal is a frame synchronization signal.

7. (Original) The system of claim 6, wherein:

each of the plurality of frames comprises a frame head and frame data;

the signal processor reads and processes the frame head when a sync signal is detected by the sync signal detector; and

the signal processor reads and processes the frame data only if the sync signal detector determines that the detected sync signal is not invalid.

8. (Currently Amended) The system of claim 1, wherein:

the received communication signal is an analog signal; and

the stored consecutive portions of the received communication signal are digital samples of the received communication signal.

9. (Currently Amended) The system of claim 1, wherein the sync signal detector monitors the read stored consecutive portions of the received communications signal to detect [[a]] the sync

signal by correlating the read stored consecutive portions of the received communications signal with the sync signal.

10. (Original) The system of claim 1, wherein the memory and the sync signal detector are implemented in a digital signal processor (DSP).

11. (Original) The system of claim 1, implemented in a communication device selected from the group consisting of: modems, mobile communication systems, hand-held communication devices, personal digital assistants (PDAs) with communication functions, cellular telephones, one-way pagers and two-way pagers.

12. (Currently Amended) A method for detecting a synchronization (sync) signal in a communication signal, comprising the steps of:

storing consecutive portions of a received communication signal in a memory;

reading the ~~consecutive~~ stored consecutive portions of the received communication signal from the memory;

monitoring the read stored consecutive portions of the received signal to detect the sync signal;

determining whether or not the sync signal detected in the read stored consecutive portions of the received communications signal is invalid; and

if the detected sync signal is invalid, then repeating the steps of reading and monitoring for previously read stored consecutive portions of the received signal.

13. (Currently Amended) The method of claim 12, further comprising the steps of reading and processing, based on the detected sync signal, stored consecutive portions of the received communication signal which are stored in the memory following the detected sync signal.

14. (Original) The method of claim 13, wherein the step of determining comprises the steps of:

monitoring a resultant processed signal from the step of processing to determine an error rate of the processed signal;

determining that the detected sync signal is invalid if the error rate exceeds a threshold; and

discontinuing the step of processing when the detected sync signal is invalid.

15. (Original) The method of claim 13, wherein:

the received communication signal comprises a plurality of frames, each comprising a frame head and frame data;

the steps of reading and processing comprise reading and processing the frame head when the sync signal is detected; and

the method further comprises the steps of, if the detected sync signal is not invalid, reading and processing the frame data.

16. (Original) The method of claim 15, wherein:

each consecutive portion of the received communication signal is a digital sample representative of the received communication signal;

the sync signal has a length of k samples; and

the steps of reading and monitoring are repeated for (k - 1) previously read samples.

17. (Currently Amended) A system for detecting a synchronization (sync) signal in a communication signal, comprising:

means for storing consecutive portions of a received communication signal; and

means for detecting the sync signal, by reading the ~~consecutive~~ stored consecutive portions of the received communication signal from the means for storing, monitoring the read stored consecutive portions of the received communications signal to detect the sync signal, and determining whether or not the sync signal detected in the read stored consecutive portions of the received communications signal is invalid, wherein the means for detecting reads and monitors previously read stored consecutive portions of the received signal from the means for storing when the detected sync signal is invalid.

18. (Currently Amended) A computer readable medium containing instructions for implementing a method for detecting a synchronization (sync) signal in a communication signal, the method comprising the steps of:

storing consecutive portions of a received communication signal in a memory;

reading the ~~consecutive~~ stored consecutive portions of the received communication signal from the memory;

monitoring the read stored consecutive portions of the received signal to detect the sync signal;

determining whether or not the sync signal detected in the stored consecutive portions of the received signal is invalid; and

if the detected sync signal is invalid, then repeating the steps of reading and monitoring for previously read stored consecutive portions of the received signal.

19. (Original) The medium of claim 18, implemented in a digital signal processor (DSP).

20. (Currently Amended) A wireless communication device comprising:

a transceiver configured to transmit and receive communication signals; and

a digital signal processor (DSP) operatively coupled to the transceiver, the DSP comprising computer software code for detecting a synchronization (sync) signal in a communication signal, by performing the functions of:

storing consecutive portions of a received communication signal in a memory;

reading the ~~consecutive~~ stored consecutive portions of the received communication signal from the memory;

monitoring the read stored consecutive portions of the received signal to detect the sync signal;

determining whether or not the sync signal detected in the read stored consecutive portions of the received communications signal is invalid; and

if the detected sync signal is invalid, then repeating the steps of reading and monitoring for previously read stored consecutive portions of the received signal.

21. (Currently Amended) The device of claim 20, wherein the transceiver is configured to ~~received~~ receive analog communication signals and convert the received analog signals to digital signal samples for storage in the memory.

22. (Original) The device of claim 20, wherein:

the transceiver comprises a communication signal receiver;

the receiver has two modes of operation, the two modes of operation comprising a sync signal search mode in which the software code for detecting a sync signal is executed and a signal decode mode in which a received signal is processed; and

the receiver remains in the sync signal search mode until the sync signal is detected, enters the decode mode when the sync signal is detected, and reverts to the sync signal search mode if the detected sync signal is determined to be invalid.

23. (Currently Amended) The device of claim 22, wherein the receiver reverts to the sync signal search mode from the decode mode when a predetermined portion of a received communications signal has been processed.

24. (Currently Amended) The wireless communications device of claim 20, wherein the device is selected from the group consisting of wireless modems, hand-held communication devices, personal digital assistants (PDAs) with communication functions, cellular telephones, one-way pagers and two-way pagers.